[Total No. of Questions - 8] [Total No. of Printed Pages - 3] (2125)

15387

M. Tech 1st Semester Examination

Design of Electronics System

EC-102

Time : 3 Hours **Max. Marks : 100**

The candidates shall limit their answers precisely within the answer-book (40 pages) issued to them and no supplementary/continuation sheet will be issued.

Note : (i) Attempt five questions in all.

(ii) All parts of a question should be answered at one place.

(iii) Answers should be brief and to-the-point and be supplemented with neat sketches.

1. (a) Implement a 8:1 demultiplexer using NAND gates only with active low enable input.

   (b) Implement a full adder circuit using 4:1 multiplexers only.

   (c) Implement following functions using minimum number of NAND gate only :

   $F_1 = \Sigma m(1, 2, 3, 4, 7, 11, 13) + d(9, 15)$

   $F_2 = \prod M (4, 5, 6, 7, 8, 12) + d (1, 2, 3)$. (5+5+10=20)

2. (a) Using JK flip flops, design a parallel counter which counts in the sequence 000, 111, 101, 110, 001, 010, 000.....

   (b) Design a circuit which convert a BCD code into self-complementary 5211 code. (10+10=20)

[P.T.O.]

3. (a) Differentiate between PAL and PLA devices. Explain how PAL device can be used to realize the binary to gray code converter.

   (b) What is a tristate logic circuit and how does it help building a tri state bus system? Discuss the advantages of this logic in reducing hardware in system implementation. (10+10=20)

4. (a) Explain the MDS diagram construction concepts with flow diagram.

   (b) List the steps for the design of next state decodes. What is the main purpose of using MSI decoders? (10+10=20)

5. (a) What is static hazard? Define static 1 hazard, static 0 hazards, and dynamic hazard? List the types of hazards. How to eliminate the hazard?

   (b) Discuss the interfacing of digital system with coaxial and fibre optics cable. (10+10=20)

6. (a) Develop the state diagram and primitive flow table for a logic system that has 2 inputs, x and y and an output z. And reduce primitive flow table. The behavior of the circuit is stated as follows: Initially x=y=0. Whenever x=1 and y = 0 then z=1, whenever x = 0 and y = 1 then z = 0. When x=y=0 or x=y=1 no change in z it remains in the previous state. The logic system has edge triggered inputs without having a clock. The logic system changes state on the rising edges of the 2 inputs. Static input values are not to have any effect in changing the z output.

   (b) Design an asynchronous sequential circuit with two inputs X and Y and with one output Z. Whenever Y is 1, input X is transferred to Z. When Y is 0, the output does not change for any change in X. (10+10=20)

7. (a) Design a magnitude comparator circuit.

   (b) What are various clocking aspects in sequential machine? What are the design steps for traditional synchronous sequential circuits? (10+10=20)

8. Explain the following:

   (i) Wired logic.

   (ii) Electromagnetic compatibility.

   (iii) Bidirectional shift register.

   (iv) Ring Counter. (4×5=20)